HYS72D128300GBR-[5/6/7]-B
HYS72D256320GBR-[5/6/7]-B
HYS72D128500HR-[7F/7]-B
HYS72D128321GBR-[5/6/7]-B

184-Pin Registered Double Data Rate SDRAM Module

Reg DIMM

DDR SDRAM

Green Product

Lead Containing Product

Memory Products

Infineon technologies

Never stop thinking.

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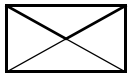


1 Overview

1.1 Features

- 184-pin Registered 8-Byte Dual-In-Line DDR SDRAM Module for “1U” PC, Workstation and Server main memory applications
- One rank 128M × 72 organization and two rank 256M × 72 organization
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR SDRAM) with a single + 2.5 V (± 0.2 V) power supply and +2.6(± 0.1 V) power supply for DDR400
- Built with DDR SDRAMs in 66-Lead TSOPII and FBGA 60 package
- Programmable CAS Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Re-drive for all input signals using register and PLL devices.
- Serial Presence Detect with E^2PROM
- Low Profile Modules form factor: 133.35 mm × 28.58 mm (1.1”) × 4.00 mm and 133.35 mm × 30.48 mm (1.2”) × 4.00 mm
- Based on Jedec standard reference card layout RawCard “B”, “C“ and “D“
- Gold plated contacts

Table 1 Performance

Part Number Speed Code			**–5**	**–6**	**–7**	**–7F**	**Unit**
Speed Grade	Component		DDR400B	DDR333B	DDR266A	DDR266	—
	Module		PC3200–3033	PC2700–2533	PC2100–2033	PC2100–2022	—
max. Clock Frequency	@ CL = 3	f_{CK3}	200	166	—	—	MHz
	@ CL = 2.5	$f_{CK2.5}$	166	166	143	143	MHz
	@ CL = 2	f_{CK2}	133	133	133	133	MHz

1.2 Description

The HYS72D[128/256][300/320/321/500][GBR/HR]-[5/6/7/7F]-B are low profile versions of the standard Registered DIMM modules with 1.1” inch (28.58) and 1.2” inch (30,40 mm) height for 1U Server Applications. The Low Profile DIMM versions are available as 128M × 72 (1 GB) and 256M × 72 (2 GB).

The memory array is designed with Double Data Rate Synchronous DRAMs for ECC applications. All control and address signals are re-driven on the DIMM using register devices and a PLL for the clock distribution. This reduces capacitive loading to the system bus, but adds one cycle to the SDRAM timing. A variety of decoupling capacitors are mounted on the PC board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

Table 2 Ordering Information[1)2)]

Type	Compliance Code	Description	SDRAM Technology
PC3200 (CL=3)			
HYS72D128300GBR–5–B	PC3200R–30331–C0	one rank 1 GByte Reg. ECC DIMM	512 MBit (×4)
HYS72D128321GBR–5–B	PC3200R–30331–B0	two ranks 1 GByte Reg. ECC DIMM	512 MBit (×8)
HYS72D256320GBR–5–B	PC3200R–30331–D0	two ranks 2 GByte Reg. ECC DIMM	512 MBit (×4)
PC2700 (CL=2.5)			
HYS72D128300GBR–6–B	PC2700R–25330–C0	one rank 1 GByte Reg. ECC DIMM	512 MBit (×4)
HYS72D128321GBR–6–B	PC2700R–25330–B0	two ranks 1 GByte Reg. ECC DIMM	512 MBit (×8)
HYS72D256320GBR–6–B	PC2700R–25330–D0	two ranks 2 GByte Reg. ECC DIMM	512 MBit (×4)
PC2100 (CL=2)			
HYS72D128300GBR–7–B	PC2100R–20330–C0	one rank 1 GByte Reg. ECC DIMM	512 MBit (×4)
HYS72D128321GBR–7–B	PC2100R–20330–B0	two ranks1 GByte Reg. ECC DIMM	512 MBit (×8)
HYS72D256320GBR–7–B	PC2100R–20330–D0	two ranks 2 GByte Reg. ECC DIMM	512 MBit (×4)
HYS72D128500HR–7F–B	PC2100R–20220–M	one rank 1GByte Reg. ECC DIMM	512 MBit (×4)
HYS72D128500HR–7–B	PC2100R–20330–M	one rank 1GByte Reg. ECC DIMM	512 MBit (×4)

1) All part numbers end with a place code (not shown), designating the silicon-die revision. Reference information available on request. Example: HYS72D128300GBR-[5/6/7]-B, indicating Rev.B die are used for SDRAM components.

2) The Compliance Code is printed on the module labels and describes the speed sort for example “PC2100R”, the latencies (for example “20330” means CAS latency = 2.5, t_{RCD} latency = 3 and t_{RP} latency =3) and the Raw Card used for this module

2 Pin Configuration

Table 3 Pin Definitions and Functions

Symbol	Type	Function
A0 - A11,A12		Address Inputs
BA0, BA1		Bank Selects
DQ0 - DQ63		Data Input/Output
CB0 - CB7		Check Bits (×72 organization only)
$\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$		Command Inputs
CKE0, CKE1		Clock Enable
DQS0 - DQS8		SDRAM low data strobes
CK0, $\overline{CK0}$		Differential Clock Input
DM0 - DM8 DQS9 - DQS17		SDRAM low data mask/ high data strobes
$\overline{S0}$ - $\overline{S1}$		Chip Selects
V_{DD}		Power (+2.5 V)
V_{SS}		Ground
V_{DDQ}		I/O Driver power supply
V_{DDID}		VDD Indentification flag
V_{DDSPD}		EEPROM power supply
V_{REF}		I/O reference supply
SCL		Serial bus clock
SDA		Serial bus data line
SA0 - SA2		slave address select
NC		no connect
DU		don’t use
RESET		Reset pin (forces register inputs low)[1)]

1) for detailed description of the Power Up and Power Management on DDR Registered DIMMs see the Application Note at the end of this datasheet

Table 4 Pin Configuration[1)]

PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
1	V_{REF}	48	A0	94	DQ4	141	A10
2	DQ0	49	CB2	95	DQ5	142	CB6
3	V_{SS}	50	V_{SS}	96	V_{DDQ}	143	V_{DDQ}
4	DQ1	51	CB3	97	DQS9	144	CB7
5	DQS0	52	BA1	98	DQ6	**KEY**	
6	DQ2	**KEY**		99	DQ7	145	V_{SS}
7	V_{DD}	53	DQ32	100	V_{SS}	146	DQ36
8	DQ3	54	V_{DDQ}	101	NC	147	DQ37
9	NC	55	DQ33	102	NC	148	V_{DD}
10	$\overline{\text{RESET}}$	56	DQS4	103	NC	149	DM4/DQS13
11	V_{SS}	57	DQ34	104	V_{DDQ}	150	DQ38
12	DQ8	58	V_{SS}	105	DQ12	151	DQ39
13	DQ9	59	BA0	106	DQ13	152	V_{SS}
14	DQS1	60	DQ35	107	DQS10	153	DQ44
15	V_{DDQ}	61	DQ40	108	V_{DD}	154	$\overline{\text{RAS}}$
16	DU	62	V_{DDQ}	109	DQ14	155	DQ45
17	DU	63	$\overline{\text{WE}}$	110	DQ15	156	V_{DDQ}
18	V_{SS}	64	DQ41	111	CKE1	157	$\overline{\text{S0}}$
19	DQ10	65	$\overline{\text{CAS}}$	112	V_{DDQ}	158	$\overline{\text{S1}}$
20	DQ11	66	V_{SS}	113	NC	159	DQS14
21	CKE0	67	DQS5	114	DQ20	160	V_{SS}
22	V_{DDQ}	68	DQ42	115	NC / A12	161	DQ46
23	DQ16	69	DQ43	116	V_{SS}	162	DQ47
24	DQ17	70	V_{DD}	117	DQ21	163	NC
25	DQS2	71	NC	118	A11	164	V_{DDQ}
26	V_{SS}	72	DQ48	119	DQS11	165	DQ52
27	A9	73	DQ49	120	V_{DD}	166	DQ53
28	DQ18	74	V_{SS}	121	DQ22	167	NC
29	A7	75	DU	122	A8	168	V_{DD}
30	V_{DDQ}	76	DU	123	DQ23	169	DQS15
31	DQ19	77	V_{DDQ}	124	V_{SS}	170	DQ54
32	A5	78	DQS6	125	A6	171	DQ55
33	DQ24	79	DQ50	126	DQ28	172	V_{DDQ}
34	V_{SS}	80	DQ51	127	DQ29	173	NC
35	DQ25	81	V_{SS}	128	V_{DDQ}	174	DQ60
36	DQS3	82	V_{DDID}	129	DQS12	175	DQ61
37	A4	83	DQ56	130	A3	176	V_{SS}
38	V_{DD}	84	DQ57	131	DQ30	177	DQS16
39	DQ26	85	V_{DD}	132	V_{SS}	178	DQ62
40	DQ27	86	DQS7	133	DQ31	179	DQ63
41	A2	87	DQ58	134	CB4	180	V_{DDQ}

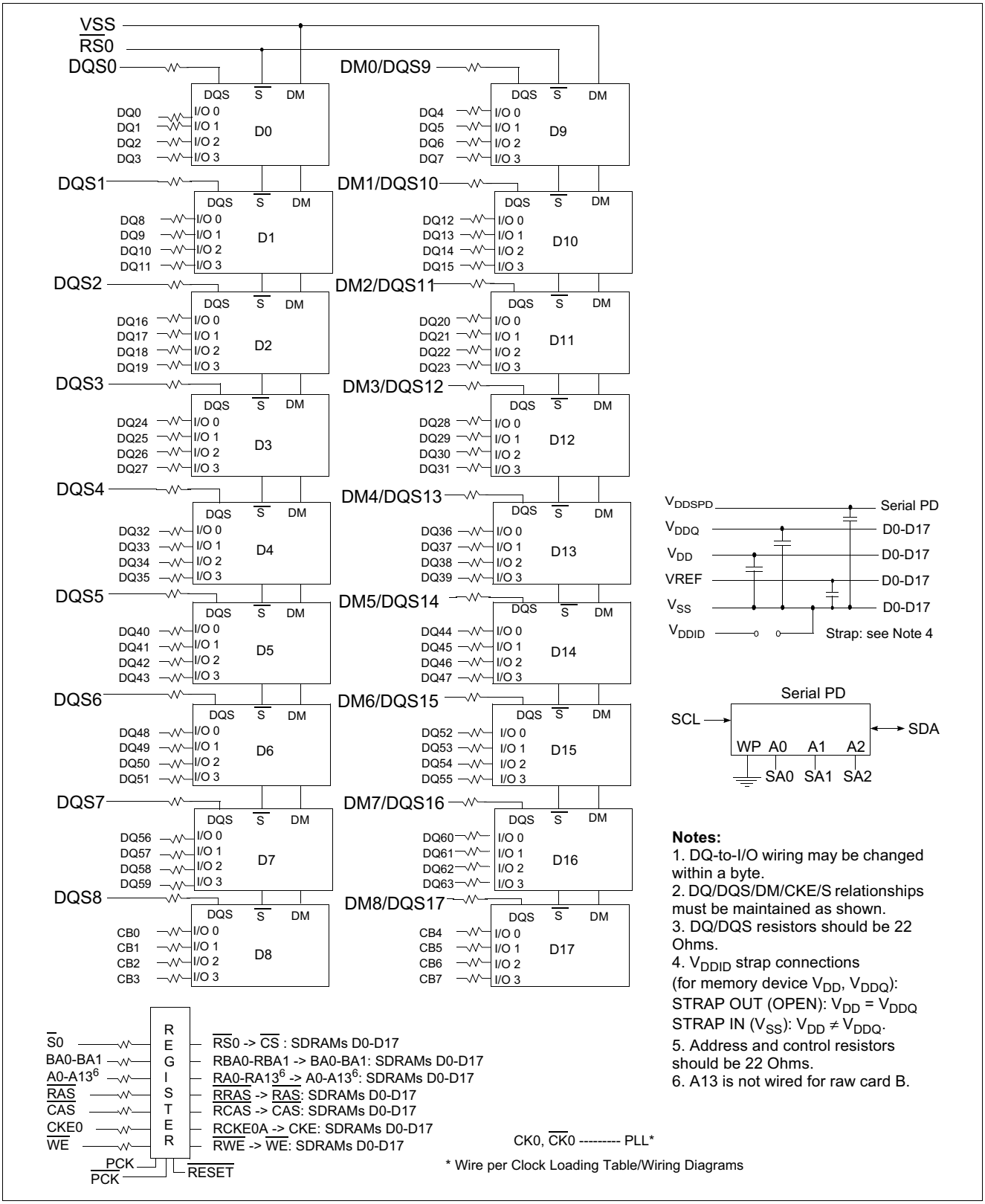
Table 4 Pin Configuration[1)] (cont'd)

PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
42	V_{SS}	88	DQ59	135	CB5	181	SA0
43	A1	89	V_{SS}	136	V_{DDQ}	182	SA1
44	CB0	90	NC	137	CK0	183	SA2
45	CB1	91	SDA	138	$\overline{CK0}$	184	V_{DDSPD}
46	V_{DD}	92	SCL	139	V_{SS}	–	–
47	DQS8	93	V_{SS}	140	DQS17	–	–

1) A12 is used for 256Mbit and 512Mbit based modules only.

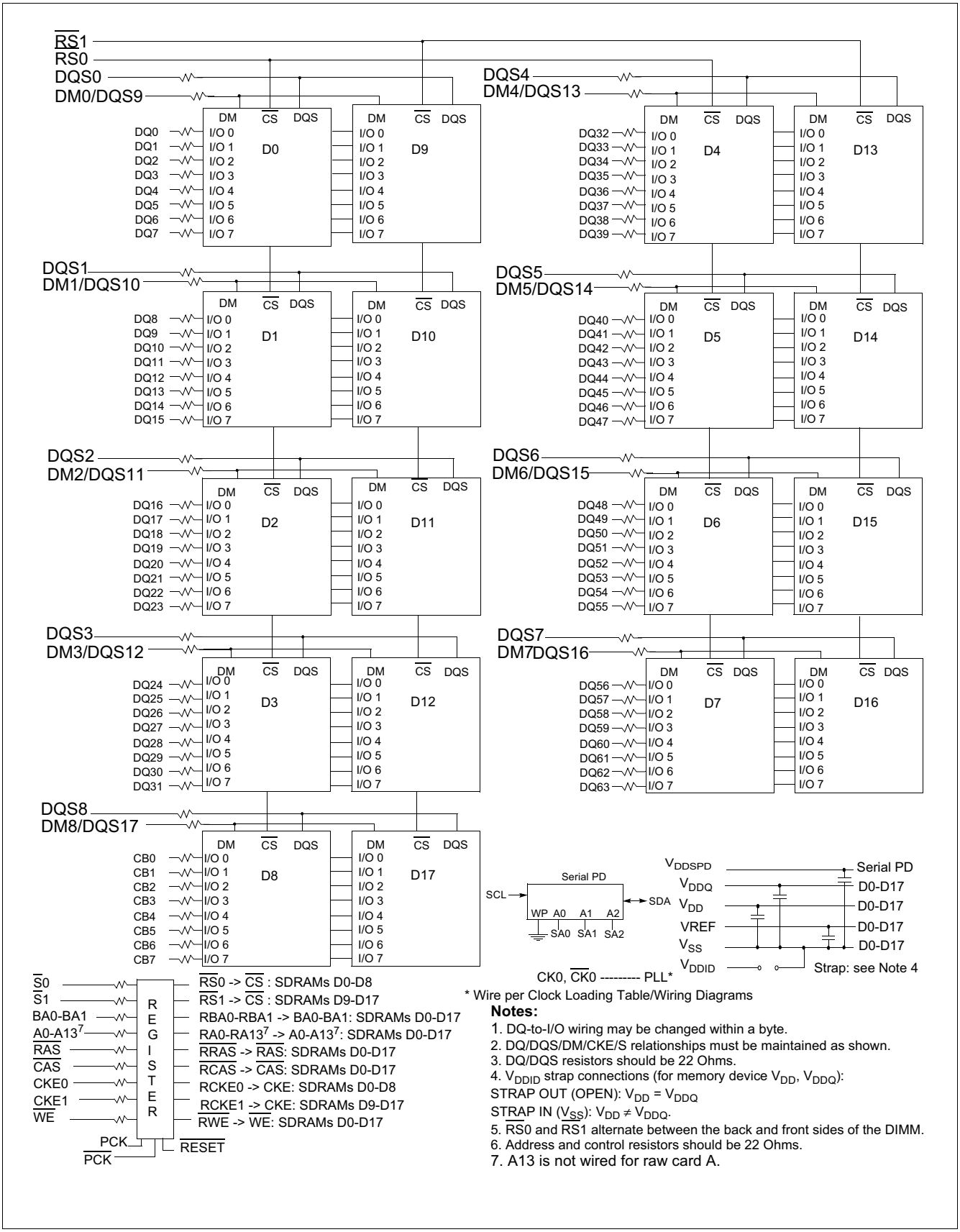
Table 5 Address Format

Density	Organization	Memory Ranks	SDRAMs	# of SDRAMs	# of row/bank/ column bits	Refresh	Period	Interval
1 GB	128M x 72	1	128M × 4	18	13/2/12	8K	64 ms	7.8 µs
1 GB	128M x 72	2	64M × 8	18	13/2/11	8K	64 ms	7.8 µs
2 GB	256M x 72	2	128M × 4	36	13/2/12	8K	64 ms	7.8 µs



Notes:
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$.
5. Address and control resistors should be 22 Ohms.
6. A13 is not wired for raw card B.

Figure 1 Block Diagram: 1 Rank 128M × 72 DDR SDRAM DIMM HYS72D128[300/500]GBR–[5/6/7/7F]–B

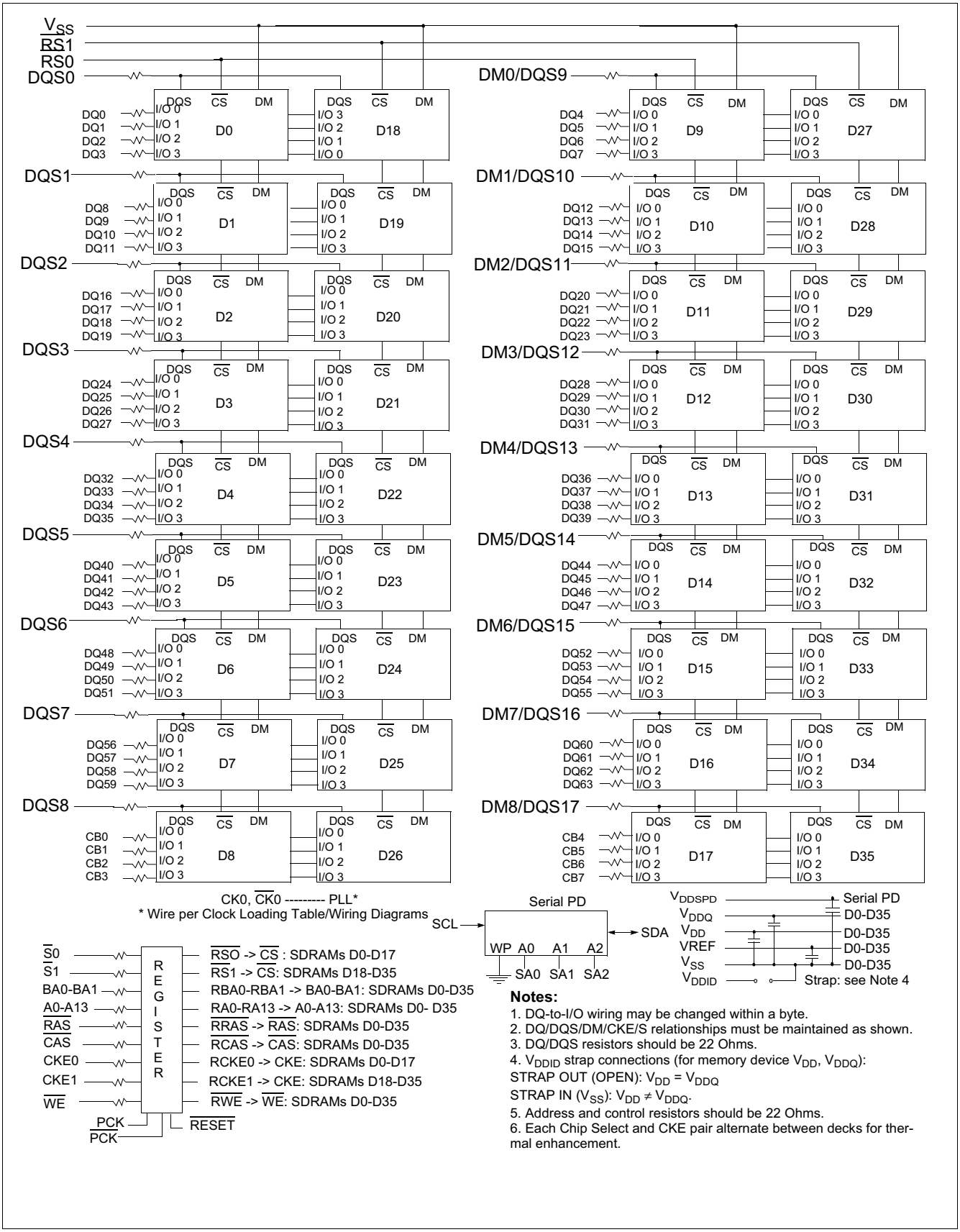


* Wire per Clock Loading Table/Wiring Diagrams

Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$.
5. RS0 and RS1 alternate between the back and front sides of the DIMM.
6. Address and control resistors should be 22 Ohms.
7. A13 is not wired for raw card A.

Figure 2 Block Diagram – 2 Ranks 64M × 72 DDR SDRAM HYS72D128321GBR-[5/6/7]–B



Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$.
5. Address and control resistors should be 22 Ohms.
6. Each Chip Select and CKE pair alternate between decks for thermal enhancement.

Figure 3 Block Diagram – 2 Ranks 128M × 72 DDR SDRAM HYS72D256320GBR-[5/6/7]–B

3 Electrical Characteristics

3.1 Operating Conditions

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Voltage on I/O pins relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	–	V_{DDQ} + 0.5	V	–
Voltage on inputs relative to V_{SS}	V_{IN}	–1	–	+3.6	V	–
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	–1	–	+3.6	V	–
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	–1	–	+3.6	V	–
Operating temperature (ambient)	T_A	0	–	+70	°C	–
Storage temperature (plastic)	T_{STG}	-55	–	+150	°C	–
Power dissipation (per SDRAM component)	P_D	–	1	–	W	–
Short circuit output current	I_{OUT}	–	50	–	mA	–

Attention: Permanent damage to the device may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only, and functional operation should be restricted to recommended operation conditions. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability and exceeding only one of the values may cause irreversible damage to the integrated circuit.

Table 7 Electrical Characteristics and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note/Test Condition [1]
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	$f_{CK} \leq 166$ MHz
Device Supply Voltage	V_{DD}	2.5	2.6	2.7	V	$f_{CK} > 166$ MHz [2]
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	$f_{CK} \leq 166$ MHz [3]
Output Supply Voltage	V_{DDQ}	2.5	2.6	2.7	V	$f_{CK} > 166$ MHz [2)3)]
EEPROM supply voltage	V_{DDSPD}	2.3	2.5	3.6	V	—
Supply Voltage, I/O Supply Voltage	V_{SS}, V_{SSQ}	0		0	V	—
Input Reference Voltage	V_{REF}	0.49 × V_{DDQ}	0.5 × V_{DDQ}	0.51 × V_{DDQ}	V	[4]
I/O Termination Voltage (System)	V_{TT}	V_{REF} – 0.04		V_{REF} + 0.04	V	[5]
Input High (Logic1) Voltage	$V_{IH(DC)}$	V_{REF} + 0.15		V_{DDQ} + 0.3	V	[8]
Input Low (Logic0) Voltage	$V_{IL(DC)}$	–0.3		V_{REF} – 0.15	V	[8]
Input Voltage Level, CK and $\overline{CK}$ Inputs	$V_{IN(DC)}$	–0.3		V_{DDQ} + 0.3	V	[8]
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID(DC)}$	0.36		V_{DDQ} + 0.6	V	[8)6)]
VI-Matching Pull-up Current to Pull-down Current	VI_{Ratio}	0.71		1.4	—	[7]

Table 7 Electrical Characteristics and DC Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition [1]
		Min.	Typ.	Max.		
Input Leakage Current	I_I	–2		2	µA	Any input 0 V $\leq V_{IN} \leq V_{DD}$; All other pins not under test = 0 V [8)9)]
Output Leakage Current	I_{OZ}	–5		5	µA	DQs are disabled; 0 V $\leq V_{OUT} \leq V_{DDQ}$
Output High Current, Normal Strength Driver	I_{OH}	—		–16.2	mA	V_{OUT} = 1.95 V
Output Low Current, Normal Strength Driver	I_{OL}	16.2		—	mA	V_{OUT} = 0.35 V

1) 0 °C $\leq T_A \leq$ 70 °C

2) DDR400 conditions apply for all clock frequencies above 166 MHz

3) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.

4) Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\ (DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.

5) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.

6) V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

7) The ratio of the pull-up current to the pull-down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0 V. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

8) Inputs are not recognized as valid until V_{REF} stabilizes.

9) Values are shown per DDR SDRAM component

Table 8 I_{DD} Conditions

Parameter	Symbol
Operating Current 0 one bank; active/ precharge; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	I_{DD0}
Operating Current 1 one bank; active/read/precharge; Burst Length = 4; see component data sheet.	I_{DD1}
Precharge Power-Down Standby Current all banks idle; power-down mode; CKE ≤ $V_{IL,MAX}$	I_{DD2P}
Precharge Floating Standby Current $\overline{CS}$ ≥ $V_{IH,,MIN}$, all banks idle; CKE ≥ $V_{IH,MIN}$; address and other control inputs changing once per clock cycle; V_{IN} = V_{REF} for DQ, DQS and DM.	I_{DD2F}
Precharge Quiet Standby Current $\overline{CS}$ ≥ V_{IHMIN}, all banks idle; CKE ≥ $V_{IH,MIN}$; V_{IN} = V_{REF} for DQ, DQS and DM; address and other control inputs stable at ≥ $V_{IH,MIN}$ or ≤ $V_{IL,MAX}$.	I_{DD2Q}
Active Power-Down Standby Current one bank active; power-down mode; CKE ≤ V_{ILMAX}; V_{IN} = V_{REF} for DQ, DQS and DM.	I_{DD3P}
Active Standby Current one bank active; $\overline{CS}$ ≥ $V_{IH,MIN}$; CKE ≥ $V_{IH,MIN}$; t_{RC} = $t_{RAS,MAX}$; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle.	I_{DD3N}
Operating Current Read one bank active; Burst Length = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B; I_{OUT} = 0 mA	I_{DD4R}
Operating Current Write one bank active; Burst Length = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B	I_{DD4W}
Auto-Refresh Current t_{RC} = t_{RFCMIN}, burst refresh	I_{DD5}
Self-Refresh Current CKE ≤ 0.2 V; external clock on	I_{DD6}
Operating Current 7 four bank interleaving with Burst Length = 4; see component data sheet.	I_{DD7}

Table 9 I_{DD} Specification for –7

Part Number & Organization	HYS72D128500HR–7F–B		HYS72D128500HR–7–B HYS72D128300GBR–7–B		HYS72D128321GBR–7–B		HYS72D256320GBR–7–B		Unit	Note 1)2)
	1 GB		1 GB		1 GB		2 GB			
	×72		×72		×72		×72			
	1 Rank		1 Rank		2 Ranks		2 Ranks			
	–7F		–7		–7		–7			
Symbol	**typ.**	**max.**	**typ.**	**max.**	**typ.**	**max.**	**typ.**	**max.**		
I_{DD0}	2158	2452	2028	2298	1587	1776	2586	2964	mA	3)
I_{DD1}	2354	2746	2208	2568	1677	1911	2766	3234	mA	3)4)
I_{DD2P}	430	448	430	448	430	448	484	520	mA	5)
I_{DD2F}	736	808	736	808	736	808	1096	1240	mA	5)
I_{DD2Q}	646	754	646	754	646	754	916	1132	mA	5)
I_{DD3P}	538	610	538	610	538	610	700	844	mA	5)
I_{DD3N}	934	1042	934	1042	934	1042	1492	1708	mA	5)
I_{DD4R}	2179	2460	2118	2388	1632	1821	2676	3054	mA	3)4)
I_{DD4W}	2273	2554	2208	2478	1677	1866	2766	3144	mA	3)
I_{DD5}	4499	5263	4278	4998	2712	3126	4836	5664	mA	3)
I_{DD6}	414	468	414	468	414	468	451	560	mA	5)
I_{DD7}	5493	6376	5088	5898	3117	3576	5646	6564	mA	3)4)

1) DRAM component currents only

2) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C

3) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as:
m × I_{DDx}[component] + **n** × I_{DD3N}[component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules

4) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions

5) The module I_{DDx} values are calculated from the corrponent I_{DDx} data sheet values as: (**m** + **n**) × I_{DDx}[component]

Table 10 I_{DD} Specification for –6

Part Number & Organization	HYS72D128300GBR–6–B		HYS72D128321GBR–6–B		HYS72D256320GBR–6–B		Unit	Note [1)2)]
	1GB		1 GB		2 GB			
	×72		×72		×72			
	1 Rank		2 Ranks		2 Ranks			
	–6		–6		–6			
Symbol	**typ.**	**max.**	**typ.**	**max.**	**typ.**	**max.**		
I_{DD0}	2350	2710	1873	2116	3016	3502	mA	3)
I_{DD1}	2620	2980	2008	2251	3286	3772	mA	3)4)
I_{DD2P}	484	502	484	502	538	574	mA	5)
I_{DD2F}	880	970	880	970	1330	1510	mA	5)
I_{DD2Q}	736	862	736	862	1042	1294	mA	5)
I_{DD3P}	628	700	628	700	826	970	mA	5)
I_{DD3N}	1096	1222	1096	1222	1762	2014	mA	5)
I_{DD4R}	2620	2980	2008	2251	3286	3772	mA	3)4)
I_{DD4W}	2710	3070	2053	2296	3376	3862	mA	3)
I_{DD5}	4690	5500	3043	3511	5356	6292	mA	3)
I_{DD6}	475	523.6	475	523.6	520	617.2	mA	5)
I_{DD7}	6310	7300	3853	4411	6976	8092	mA	3)4)

1) DRAM component currents only

2) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C

3) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as:
m × I_{DDx}[component] + **n** × I_{DD3N}[component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules

4) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions

5) The module I_{DDx} values are calculated from the corrponent I_{DDx} data sheet values as: (**m** + **n**) × I_{DDx}[component]

Table 11 I_{DD} Specification for –5

Part Number & Organization	HYS72D128300GBR–5–B		HYS72D128321GBR–5–B		HYS72D256320GBR–5–B		Unit	Note [1)2)]
	1 GB		1 GB		2 GB			
	×72		×72		×72			
	1 Rank		2 Ranks		2 Ranks			
	–5		–5		–5			
Symbol	**typ.**	**max.**	**typ.**	**max.**	**typ.**	**max.**		
I_{DD0}	2680	3040	3436	3940	3436	3940	mA	3)
I_{DD1}	2950	3400	3706	4300	3706	4300	mA	3)4)
I_{DD2P}	698	734	752	824	752	824	mA	5)
I_{DD2F}	1184	1292	1724	1940	1724	1940	mA	5)
I_{DD2Q}	986	1112	1328	1580	1328	1580	mA	5)
I_{DD3P}	860	932	1076	1220	1076	1220	mA	5)
I_{DD3N}	1400	1544	2156	2444	2156	2444	mA	5)
I_{DD4R}	3040	3490	3796	4390	3796	4390	mA	3)4)
I_{DD4W}	3130	3580	3886	4480	3886	4480	mA	3)
I_{DD5}	5290	6190	6046	7090	6046	7090	mA	3)
I_{DD6}	696.2	737.6	748.4	831.2	748.4	831.2	mA	5)
I_{DD7}	7090	8260	7846	9160	7846	9160	mA	3)4)

1) DRAM component currents only

2) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C

3) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as:
m × I_{DDx}[component] + **n** × I_{DD3N}[component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules

4) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions

5) The module I_{DDx} values are calculated from the corrponent I_{DDx} data sheet values as: (**m** + **n**) × I_{DDx}[component]

Table 12 AC Timing - Absolute Specifications –6/–5

Parameter	Symbol	–5		–6		Unit	Note/ Test Condition [1]
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	–0.6	+0.6	–0.7	+0.7	ns	2)3)4)5)
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–0.5	+0.5	–0.6	+0.6	ns	2)3)4)5)
CK high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
CK low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
Clock Half Period	t_{HP}	min. (t_{CL}, t_{CH})		min. (t_{CL}, t_{CH})		ns	2)3)4)5)
Clock cycle time	t_{CK}	5	12	—	—	ns	CL = 3.0 2)3)4)5)
		6	12	6	12	ns	CL = 2.5 2)3)4)5)
		7.5	12	7.5	12	ns	CL = 2.0 2)3)4)5)
DQ and DM input hold time	t_{DH}	0.4	—	0.45	—	ns	2)3)4)5)
DQ and DM input setup time	t_{DS}	0.4	—	0.45	—	ns	2)3)4)5)
Control and Addr. input pulse width (each input)	t_{IPW}	2.2	—	2.2	—	ns	2)3)4)5)6)
DQ and DM input pulse width (each input)	t_{DIPW}	1.75	—	1.75	—	ns	2)3)4)5)6)
Data-out high-impedance time from CK/$\overline{CK}$	t_{HZ}	–0.6	+0.6	–0.7	+0.7	ns	2)3)4)5)7)
Data-out low-impedance time from CK/$\overline{CK}$	t_{LZ}	–0.6	+0.6	–0.7	+0.7	ns	2)3)4)5)7)
Write command to 1st DQS latching transition	t_{DQSS}	0.75	1.25	0.75	1.25	t_{CK}	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.40	—	+0.40	ns	TFBGA 2)3)4)5)
		—	+0.40	—	+0.45	ns	TSOPII 2)3)4)5)
Data hold skew factor	t_{QHS}	—	+0.50	—	+0.50	ns	TFBGA 2)3)4)5)
		—	+0.50	—	+0.55	ns	TSOPII 2)3)4)5)
DQ/DQS output hold time	t_{QH}	$t_{HP} - t_{QHS}$		$t_{HP} - t_{QHS}$		ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	2)3)4)5)
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	2)3)4)5)
Write preamble setup time	t_{WPRES}	0	—	0	—	ns	2)3)4)5)8)
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)9)
Write preamble	t_{WPRE}	0.25	—	0.25	—	t_{CK}	2)3)4)5)
Address and control input setup time	t_{IS}	0.6	—	0.75	—	ns	fast slew rate 3)4)5)6)10)
		0.7	—	0.8	—	ns	slow slew rate 3)4)5)6)10)
Address and control input hold time	t_{IH}	0.6	—	0.75	—	ns	fast slew rate 3)4)5)6)10)
		0.7	—	0.8	—	ns	slow slew rate 3)4)5)6)10)
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	2)3)4)5)
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)

Table 12 AC Timing - Absolute Specifications –6/–5 (cont'd)

Parameter	Symbol	–5		–6		Unit	Note/ Test Condition [1]
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
Active to Precharge command	t_{RAS}	40	70E+3	42	70E+3	ns	2)3)4)5)
Active to Active/Auto-refresh command period	t_{RC}	55	—	60	—	ns	2)3)4)5)
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	65	—	72	—	ns	2)3)4)5)
Active to Read or Write delay	t_{RCD}	15	—	18	—	ns	2)3)4)5)
Precharge command period	t_{RP}	15	—	18	—	ns	2)3)4)5)
Active to Autoprecharge delay	t_{RAP}	15	—	18	—	ns	2)3)4)5)
Active bank A to Active bank B command	t_{RRD}	10	—	12	—	ns	2)3)4)5)
Write recovery time	t_{WR}	15	—	15	—	ns	2)3)4)5)
Auto precharge write recovery + precharge time	t_{DAL}	$(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$		$(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$		t_{CK}	2)3)4)5)11)
Internal write to read command delay	t_{WTR}	1	—	1	—	t_{CK}	2)3)4)5)
Exit self-refresh to non-read command	t_{XSNR}	75	—	75	—	ns	2)3)4)5)
Exit self-refresh to read command	t_{XSRD}	200	—	200	—	t_{CK}	2)3)4)5)
Average Periodic Refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	2)3)4)5)12)

1) 0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5 V ± 0.2 V, V_{DD} = +2.5 V ± 0.2 V (DDR333); V_{DDQ} = 2.6 V ± 0.1 V, V_{DD} = +2.6 V ± 0.1 V (DDR400)

2) Input slew rate ≥ 1 V/ns for DDR400, DDR333

3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.

4) Inputs are not recognized as valid until V_{REF} stabilizes.

5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT}.

6) These parameters guarantee device timing, but they are not necessarily tested on each device.

7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

8) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.

9) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

10) Fast slew rate ≥ 1.0 V/ns , slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{OH(ac)}$ and $V_{OL(ac)}$.

11) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.

12) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.

Table 13 AC Timing - Absolute Specifications –7/–7F

Parameter	Symbol	–7F		–7		Unit	Note/ Test Condition 1)1)
		DDR266		DDR266A			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	–0.75	+0.75	–0.75	+0.75	ns	2)2)3)3)4)4)5)5)
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–0.75	+0.75	–0.75	+0.75	ns	2)3)4)5)
CK high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
CK low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
Clock Half Period	t_{HP}	min. (t_{CL}, t_{CH})		min. (t_{CL}, t_{CH})		ns	2)3)4)5)
Clock cycle time	t_{CK}	7.5	12	7.5	12	ns	CL = 2.5 2)3)4)5)
		7.5	12	7.5	12	ns	CL = 2.0 2)3)4)5)
DQ and DM input hold time	t_{DH}	0.5	—	0.5	—	ns	2)3)4)5)
DQ and DM input setup time	t_{DS}	0.5	—	0.5	—	ns	2)3)4)5)
Control and Addr. input pulse width (each input)	t_{IPW}	2.2	—	2.2	—	ns	2)3)4)5)6)
DQ and DM input pulse width (each input)	t_{DIPW}	1.75	—	1.75	—	ns	2)3)4)5)6)
Data-out high-impedance time from CK/$\overline{CK}$	t_{HZ}	–0.75	+0.75	–0.75	+0.75	ns	2)3)4)5)7)
Data-out low-impedance time from CK/$\overline{CK}$	t_{LZ}	–0.75	+0.75	–0.75	+0.75	ns	2)3)4)5)7)
Write command to 1st DQS latching transition	t_{DQSS}	0.75	1.25	0.75	1.25	t_{CK}	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.5	—	+0.5	ns	TFBGA 2)3)4)5)
		—	+0.5	—	+0.5	ns	TSOPII 2)3)4)5)
Data hold skew factor	t_{QHS}	—	+0.75	—	+0.75	ns	TFBGA 2)3)4)5)
		—	+0.75	—	+0.75	ns	TSOPII 2)3)4)5)
DQ/DQS output hold time	t_{QH}	$t_{HP} - t_{QHS}$		$t_{HP} - t_{QHS}$		ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	2)3)4)5)
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	2)3)4)5)
Write preamble setup time	t_{WPRES}	0	—	0	—	ns	2)3)4)5)8)
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)9)
Write preamble	t_{WPRE}	0.25	—	0.25	—	t_{CK}	2)3)4)5)
Address and control input setup time	t_{IS}	0.9	—	0.9	—	ns	fast slew rate 3)4)5)6)10)
		0.9	—	0.9	—	ns	slow slew rate 3)4)5)6)10)

Table 13 AC Timing - Absolute Specifications –7/–7F

Parameter	Symbol	–7F		–7		Unit	Note/ Test Condition 1)1)
		DDR266		DDR266A			
		Min.	Max.	Min.	Max.		
Address and control input hold time	t_{IH}	0.9	—	0.9	—	ns	fast slew rate 3)4)5)6)10)
		1.0	—	1.0	—	ns	slow slew rate 3)4)5)6)10)
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	2)3)4)5)
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)
Active to Precharge command	t_{RAS}	45	120E+3	45	120E+3	ns	2)3)4)5)
Active to Active/Auto-refresh command period	t_{RC}	65	—	65	—	ns	2)3)4)5)
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	75	—	75	—	ns	2)3)4)5)
Active to Read or Write delay	t_{RCD}	20	—	20	—	ns	2)3)4)5)
Precharge command period	t_{RP}	20	—	20	—	ns	2)3)4)5)
Active to Autoprecharge delay	t_{RAP}	20	—	20	—	ns	2)3)4)5)
Active bank A to Active bank B command	t_{RRD}	15	—	15	—	ns	2)3)4)5)
Write recovery time	t_{WR}	15	—	15	—	ns	2)3)4)5)
Auto precharge write recovery + precharge time	t_{DAL}	$(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$		$(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$		t_{CK}	2)3)4)5)11)
Internal write to read command delay	t_{WTR}	1	—	1	—	t_{CK}	2)3)4)5)
Exit self-refresh to non-read command	t_{XSNR}	75	—	75	—	ns	2)3)4)5)
Exit self-refresh to read command	t_{XSRD}	200	—	200	—	t_{CK}	2)3)4)5)
Average Periodic Refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	2)3)4)5)12)

1) 0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5 V ± 0.2 V, V_{DD} = +2.5 V ± 0.2 V (DDR333); V_{DDQ} = 2.6 V ± 0.1 V, V_{DD} = +2.6 V ± 0.1 V (DDR400)

2) Input slew rate ≥ 1 V/ns for DDR400, DDR333

3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.

4) Inputs are not recognized as valid until V_{REF} stabilizes.

5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT}.

6) These parameters guarantee device timing, but they are not necessarily tested on each device.

7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

8) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.

9) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

10) Fast slew rate ≥ 1.0 V/ns , slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{OH(ac)}$ and $V_{OL(ac)}$.

11) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.

12) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.

4 SPD Contents

Table 14 SPD Codes for HYS72D[128/256][300/321/320]GBR–5–B

	Part Number & Organization	HYS72D128300GBR–5–B	HYS72D128321GBR–5–B	HYS72D256320GBR–5–B
		1 GB	1 GB	2 GB
		×72	×72	×72
		1 Rank	2 Ranks	2 Ranks
		–5	–5	–5
	Label Code	**PC3200R–30331**	**PC3200R–30331**	**PC3200R–30331**
	JEDEC SPD Revision	**Rev. 1.0**	**Rev. 1.0**	**Rev. 1.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in E2PROM	80	80	80
1	Total number of Bytes in E2PROM	08	08	08
2	Memory Type (DDR = 07h)	07	07	07
3	Number of Row Addresses	0D	0D	0D
4	Number of Column Addresses	0C	0B	0C
5	Number of DIMM Ranks	01	02	02
6	Data Width (LSB)	48	48	48
7	Data Width (MSB)	00	00	00
8	Interface Voltage Levels	04	04	04
9	tCK @ CLmax (Byte 18) [ns]	50	50	50
10	tAC SDRAM @ CLmax (Byte 18) [ns]	50	50	50
11	Error Correction Support (non- / ECC)	02	02	02
12	Refresh Rate	82	82	82
13	Primary SDRAM Width	04	08	04
14	Error Checking SDRAM Width	04	08	04
15	tCCD [cycles]	01	01	01
16	Burst Length Supported	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04
18	CAS Latency	1C	1C	1C
19	CS Latency	01	01	01
20	Write Latency	02	02	02
21	DIMM Attributes	26	26	26
22	Component Attributes	C1	C1	C1
23	tCK @ CLmax -0.5 (Byte 18) [ns]	60	60	60
24	tAC SDRAM @ CLmax -0.5 [ns]	50	50	50
25	tCK @ CLmax -1 (Byte 18) [ns]	75	75	75

Table 14 SPD Codes for HYS72D[128/256][300/321/320]GBR–5–B

	Part Number & Organization	HYS72D128300GBR–5–B	HYS72D128321GBR–5–B	HYS72D256320GBR–5–B
		1 GB	1 GB	2 GB
		×72	×72	×72
		1 Rank	2 Ranks	2 Ranks
		–5	–5	–5
	Label Code	**PC3200R–30331**	**PC3200R–30331**	**PC3200R–30331**
	JEDEC SPD Revision	**Rev. 1.0**	**Rev. 1.0**	**Rev. 1.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
26	tAC SDRAM @ CLmax -1 [ns]	50	50	50
27	tRPmin [ns]	3C	3C	3C
28	tRRDmin [ns]	28	28	28
29	tRCDmin [ns]	3C	3C	3C
30	tRASmin [ns]	28	28	28
31	Module Density per Rank	01	80	01
32	tAS, tCS [ns]	60	60	60
33	tAH, TCH [ns]	60	60	60
34	tDS [ns]	40	40	40
35	tDH [ns]	40	40	40
36 – 40	not used	00	00	00
41	tRCmin [ns]	37	37	37
42	tRFCmin [ns]	41	41	41
43	tCKmax [ns]	28	28	28
44	tDQSQmax [ns]	28	28	28
45	tQHSmax [ns]	50	50	50
46	not used	00	00	00
47	DIMM PCB Height	01	01	01
48 – 61	not used	00	00	00
62	SPD Revision	10	10	10
63	Checksum of Byte 0-62	E1	68	E2
64	JEDEC ID Code of Infineon (1)	C1	C1	C1
65 – 71	JEDEC ID Code of Infineon (2)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Part Number, Char 1	37	37	37
74	Part Number, Char 2	32	32	32
75	Part Number, Char 3	44	44	44

Table 14 SPD Codes for HYS72D[128/256][300/321/320]GBR–5–B

	Part Number & Organization	HYS72D128300GBR–5–B	HYS72D128321GBR–5–B	HYS72D256320GBR–5–B
		1 GB	1 GB	2 GB
		×72	×72	×72
		1 Rank	2 Ranks	2 Ranks
		–5	–5	–5
	Label Code	**PC3200R–30331**	**PC3200R–30331**	**PC3200R–30331**
	JEDEC SPD Revision	**Rev. 1.0**	**Rev. 1.0**	**Rev. 1.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
76	Part Number, Char 4	31	31	32
77	Part Number, Char 5	32	32	35
78	Part Number, Char 6	38	38	36
79	Part Number, Char 7	33	33	33
80	Part Number, Char 8	30	32	32
81	Part Number, Char 9	30	31	30
82	Part Number, Char 10	47	47	47
83	Part Number, Char 11	42	42	42
84	Part Number, Char 12	52	52	52
85	Part Number, Char 13	35	35	35
86	Part Number, Char 14	42	42	42
87	Part Number, Char 15	20	20	20
88	Part Number, Char 16	20	20	20
89	Part Number, Char 17	20	20	20
90	Part Number, Char 18	20	20	20
91	Module Revision Code	xx	xx	xx
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 – 98	Module Serial Number (1 - 4)	xx	xx	xx
99 – 127	not used	00	00	00

Table 15 SPD Codes for HYS72D[128/256][300/321/320]GBR–6–B

	Part Number & Organization	HYS72D128300GBR–6–B	HYS72D128321GBR–6–B	HYS72D256320GBR–6–B
		1 GB	1 GB	2 GB
		×72	×72	×72
		1 Rank	2 Ranks	2 Ranks
		–6	–6	–6
	Label Code	**PC2700R–25330**	**PC2700R–25330**	**PC2700R–25330**
	Jedec SPD Revision	**Rev. 0.0**	**Rev. 0.0**	**Rev. 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in E2PROM	80	80	80
1	Total number of Bytes in E2PROM	08	08	08
2	Memory Type (DDR = 07h)	07	07	07
3	Number of Row Addresses	0D	0D	0D
4	Number of Column Addresses	0C	0B	0C
5	Number of DIMM Ranks	01	02	02
6	Data Width (LSB)	48	48	48
7	Data Width (MSB)	00	00	00
8	Interface Voltage Levels	04	04	04
9	tCK @ CLmax (Byte 18) [ns]	60	60	60
10	tAC SDRAM @ CLmax (Byte 18) [ns]	70	70	70
11	Error Correction Support (non- / ECC)	02	02	02
12	Refresh Rate	82	82	82
13	Primary SDRAM Width	04	08	04
14	Error Checking SDRAM Width	04	08	04
15	tCCD [cycles]	01	01	01
16	Burst Length Supported	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04
18	CAS Latency	0C	0C	0C
19	CS Latency	01	01	01
20	Write Latency	02	02	02
21	DIMM Attributes	26	26	26
22	Component Attributes	C1	C1	C1
23	tCK @ CLmax -0.5 (Byte 18) [ns]	75	75	75
24	tAC SDRAM @ CLmax -0.5 [ns]	70	70	70
25	tCK @ CLmax -1 (Byte 18) [ns]	00	00	00

Table 15 SPD Codes for HYS72D[128/256][300/321/320]GBR–6–B

	Part Number & Organization	HYS72D128300GBR–6–B	HYS72D128321GBR–6–B	HYS72D256320GBR–6–B
		1 GB	1 GB	2 GB
		×72	×72	×72
		1 Rank	2 Ranks	2 Ranks
		–6	–6	–6
	Label Code	**PC2700R–25330**	**PC2700R–25330**	**PC2700R–25330**
	Jedec SPD Revision	**Rev. 0.0**	**Rev. 0.0**	**Rev. 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
26	tAC SDRAM @ CLmax -1 [ns]	00	00	00
27	tRPmin [ns]	48	48	48
28	tRRDmin [ns]	30	30	30
29	tRCDmin [ns]	48	48	48
30	tRASmin [ns]	2A	2A	2A
31	Module Density per Rank	01	80	01
32	tAS, tCS [ns]	75	75	75
33	tAH, TCH [ns]	75	75	75
34	tDS [ns]	45	45	45
35	tDH [ns]	45	45	45
36 – 40	not used	00	00	00
41	tRCmin [ns]	3C	3C	3C
42	tRFCmin [ns]	48	48	48
43	tCKmax [ns]	30	30	30
44	tDQSQmax [ns]	28	28	28
45	tQHSmax [ns]	50	50	50
46	not used	00	00	00
47	DIMM PCB Height	00	00	00
48 – 61	not used	00	00	00
62	SPD Revision	00	00	00
63	Checksum of Byte 0-62	CA	51	CB
64	JEDEC ID Code of Infineon (1)	C1	C1	C1
65 – 71	JEDEC ID Code of Infineon (2 - 8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Part Number, Char 1	37	37	37
74	Part Number, Char 2	32	32	32
75	Part Number, Char 3	44	44	44

Table 15 SPD Codes for HYS72D[128/256][300/321/320]GBR–6–B

	Part Number & Organization	HYS72D128300GBR–6–B	HYS72D128321GBR–6–B	HYS72D256320GBR–6–B
		1 GB	1 GB	2 GB
		×72	×72	×72
		1 Rank	2 Ranks	2 Ranks
		–6	–6	–6
	Label Code	**PC2700R–25330**	**PC2700R–25330**	**PC2700R–25330**
	Jedec SPD Revision	**Rev. 0.0**	**Rev. 0.0**	**Rev. 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
76	Part Number, Char 4	31	31	32
77	Part Number, Char 5	32	32	35
78	Part Number, Char 6	38	38	36
79	Part Number, Char 7	33	33	33
80	Part Number, Char 8	30	32	32
81	Part Number, Char 9	30	31	30
82	Part Number, Char 10	47	47	47
83	Part Number, Char 11	42	42	42
84	Part Number, Char 12	52	52	52
85	Part Number, Char 13	36	36	36
86	Part Number, Char 14	42	42	42
87	Part Number, Char 15	20	20	20
88	Part Number, Char 16	20	20	20
89	Part Number, Char 17	20	20	20
90	Part Number, Char 18	20	20	20
91	Module Revision Code	xx	xx	xx
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 – 98	Module Serial Number (1 - 4)	xx	xx	xx
99 – 127	not used	00	00	00

Table 16 SPD Codes for HYS72D[128/256][300/321/320]GBR–7–B

	Part Number & Organization	HYS72D128300GBR–7–B	HYS72D128321GBR–7–B	HYS72D256320GBR–7–B
		1 GB	1 GB	2 GB
		×72	×72	×72
		1 Rank	2 Ranks	2 Ranks
		reg	reg	reg
	Label Code	**PC2100R–20330**	**PC2100R–20330**	**PC2100R–20330**
	Jedec SPD Revision	**Rev. 0.0**	**Rev. 0.0**	**Rev. 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in E2PROM	80	80	80
1	Total number of Bytes in E2PROM	08	08	08
2	Memory Type (DDR = 07h)	07	07	07
3	Number of Row Addresses	0D	0D	0D
4	Number of Column Addresses	0C	0B	0C
5	Number of DIMM Ranks	01	02	02
6	Data Width (LSB)	48	48	48
7	Data Width (MSB)	00	00	00
8	Interface Voltage Levels	04	04	04
9	tCK @ CLmax (Byte 18) [ns]	70	70	70
10	tAC SDRAM @ CLmax (Byte 18) [ns]	75	75	75
11	Error Correction Support (non- / ECC)	02	02	02
12	Refresh Rate	82	82	82
13	Primary SDRAM Width	04	08	04
14	Error Checking SDRAM Width	04	08	04
15	tCCD [cycles]	01	01	01
16	Burst Length Supported	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04
18	CAS Latency	0C	0C	0C
19	CS Latency	01	01	01
20	Write Latency	02	02	02
21	DIMM Attributes	26	26	26
22	Component Attributes	C1	C1	C1
23	tCK @ CLmax -0.5 (Byte 18) [ns]	75	75	75
24	tAC SDRAM @ CLmax -0.5 [ns]	75	75	75
25	tCK @ CLmax -1 (Byte 18) [ns]	00	00	00

Table 16 SPD Codes for HYS72D[128/256][300/321/320]GBR–7–B

	Part Number & Organization	HYS72D128300GBR–7–B	HYS72D128321GBR–7–B	HYS72D256320GBR–7–B
		1 GB	1 GB	2 GB
		×72	×72	×72
		1 Rank	2 Ranks	2 Ranks
		reg	reg	reg
	Label Code	**PC2100R–20330**	**PC2100R–20330**	**PC2100R–20330**
	Jedec SPD Revision	**Rev. 0.0**	**Rev. 0.0**	**Rev. 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
26	tAC SDRAM @ CLmax -1 [ns]	00	00	00
27	tRPmin [ns]	50	50	50
28	tRRDmin [ns]	3C	3C	3C
29	tRCDmin [ns]	50	50	50
30	tRASmin [ns]	2D	2D	2D
31	Module Density per Rank	01	80	01
32	tAS, tCS [ns]	90	90	90
33	tAH, TCH [ns]	90	90	90
34	tDS [ns]	50	50	50
35	tDH [ns]	50	50	50
36 – 40	not used	00	00	00
41	tRCmin [ns]	41	41	41
42	tRFCmin [ns]	4B	4B	4B
43	tCKmax [ns]	30	30	30
44	tDQSQmax [ns]	32	32	32
45	tQHSmax [ns]	75	75	75
46	not used	00	00	00
47	DIMM PCB Height	00	00	00
48 – 61	not used	00	00	00
62	SPD Revision	00	00	00
63	Checksum of Byte 0-62	86	0D	87
64	JEDEC ID Code of Infineon (1)	C1	C1	C1
65 – 71	JEDEC ID Code of Infineon (2 - 8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Part Number, Char 1	37	37	37
74	Part Number, Char 2	32	32	32
75	Part Number, Char 3	44	44	44

Table 16 SPD Codes for HYS72D[128/256][300/321/320]GBR–7–B

	Part Number & Organization	HYS72D128300GBR–7–B	HYS72D128321GBR–7–B	HYS72D256320GBR–7–B
		1 GB	1 GB	2 GB
		×72	×72	×72
		1 Rank	2 Ranks	2 Ranks
		reg	reg	reg
	Label Code	**PC2100R–20330**	**PC2100R–20330**	**PC2100R–20330**
	Jedec SPD Revision	**Rev. 0.0**	**Rev. 0.0**	**Rev. 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
76	Part Number, Char 4	31	31	32
77	Part Number, Char 5	32	32	35
78	Part Number, Char 6	38	38	36
79	Part Number, Char 7	33	33	33
80	Part Number, Char 8	30	32	32
81	Part Number, Char 9	30	31	30
82	Part Number, Char 10	47	47	47
83	Part Number, Char 11	42	42	42
84	Part Number, Char 12	52	52	52
85	Part Number, Char 13	37	37	37
86	Part Number, Char 14	42	42	42
87	Part Number, Char 15	20	20	20
88	Part Number, Char 16	20	20	20
89	Part Number, Char 17	20	20	20
90	Part Number, Char 18	20	20	20
91	Module Revision Code	xx	xx	xx
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 – 98	Module Serial Number (1 - 4)	xx	xx	xx
99 – 127	not used	00	00	00

Table 17 SPD Codes for HYS72D128500HR–[7F/7]–B

	Part Number & Organization	HYS72D128500HR–7F–B	HYS72D128500HR–7–B
		1 GB	**1 GB**
		×72	**×72**
		1 Rank	**1 Rank**
		reg	**reg**
	Label Code	**PC2100R–20220**	**PC2100R–20330**
	Jedec SPD Revision	**Rev. 0.0**	**Rev. 0.0**
Byte#	**Description**	**HEX**	**HEX**
0	Programmed SPD Bytes in E2PROM	80	80
1	Total number of Bytes in E2PROM	08	08
2	Memory Type (DDR = 07h)	07	07
3	Number of Row Addresses	0D	0D
4	Number of Column Addresses	0C	0C
5	Number of DIMM Ranks	01	01
6	Data Width (LSB)	48	48
7	Data Width (MSB)	00	00
8	Interface Voltage Levels	04	04
9	tCK @ CLmax (Byte 18) [ns]	70	70
10	tAC SDRAM @ CLmax (Byte 18) [ns]	75	75
11	Error Correction Support (non- / ECC)	02	02
12	Refresh Rate	82	82
13	Primary SDRAM Width	04	04
14	Error Checking SDRAM Width	04	04
15	tCCD [cycles]	01	01
16	Burst Length Supported	0E	0E
17	Number of Banks on SDRAM Device	04	04
18	CAS Latency	0C	0C
19	CS Latency	01	01
20	Write Latency	02	02
21	DIMM Attributes	26	26
22	Component Attributes	C1	C1
23	tCK @ CLmax -0.5 (Byte 18) [ns]	75	75
24	tAC SDRAM @ CLmax -0.5 [ns]	75	75
25	tCK @ CLmax -1 (Byte 18) [ns]	00	00

Table 17 SPD Codes for HYS72D128500HR–[7F/7]–B

	Part Number & Organization	HYS72D128500HR–7F–B	HYS72D128500HR–7–B
		1 GB	1 GB
		×72	×72
		1 Rank	1 Rank
		reg	reg
	Label Code	**PC2100R–20220**	**PC2100R–20330**
	Jedec SPD Revision	**Rev. 0.0**	**Rev. 0.0**
Byte#	**Description**	**HEX**	**HEX**
26	tAC SDRAM @ CLmax -1 [ns]	00	00
27	tRPmin [ns]	3C	50
28	tRRDmin [ns]	3C	3C
29	tRCDmin [ns]	3C	50
30	tRASmin [ns]	2D	2D
31	Module Density per Rank	01	01
32	tAS, tCS [ns]	90	90
33	tAH, TCH [ns]	90	90
34	tDS [ns]	50	50
35	tDH [ns]	50	50
36 – 40	not used	00	00
41	tRCmin [ns]	3C	41
42	tRFCmin [ns]	4B	4B
43	tCKmax [ns]	30	30
44	tDQSQmax [ns]	32	32
45	tQHSmax [ns]	75	75
46	not used	00	00
47	DIMM PCB Height	00	00
48 – 61	not used	00	00
62	SPD Revision	00	00
63	Checksum of Byte 0-62	59	86
64	JEDEC ID Code of Infineon (1)	C1	C1
65 – 71	JEDEC ID Code of Infineon (2 – 8)	00	00
72	Module Manufacturer Location	xx	xx
73	Part Number, Char 1	37	37
74	Part Number, Char 2	32	32
75	Part Number, Char 3	44	44

Table 17 SPD Codes for HYS72D128500HR–[7F/7]–B

	Part Number & Organization	HYS72D128500HR–7F–B	HYS72D128500HR–7–B
		1 GB	1 GB
		×72	×72
		1 Rank	1 Rank
		reg	reg
	Label Code	**PC2100R–20220**	**PC2100R–20330**
	Jedec SPD Revision	**Rev. 0.0**	**Rev. 0.0**
Byte#	**Description**	**HEX**	**HEX**
76	Part Number, Char 4	31	31
77	Part Number, Char 5	32	32
78	Part Number, Char 6	38	38
79	Part Number, Char 7	35	35
80	Part Number, Char 8	30	30
81	Part Number, Char 9	30	30
82	Part Number, Char 10	48	48
83	Part Number, Char 11	52	52
84	Part Number, Char 12	37	37
85	Part Number, Char 13	46	42
86	Part Number, Char 14	42	20
87	Part Number, Char 15	20	20
88	Part Number, Char 16	20	20
89	Part Number, Char 17	20	20
90	Part Number, Char 18	20	20
91	Module Revision Code	xx	xx
92	Test Program Revision Code	xx	xx
93	Module Manufacturing Date Year	xx	xx
94	Module Manufacturing Date Week	xx	xx
95 – 98	Module Serial Number (1 – 4)	xx	xx
99 – 127	not used	00	00

5 Package Outlines

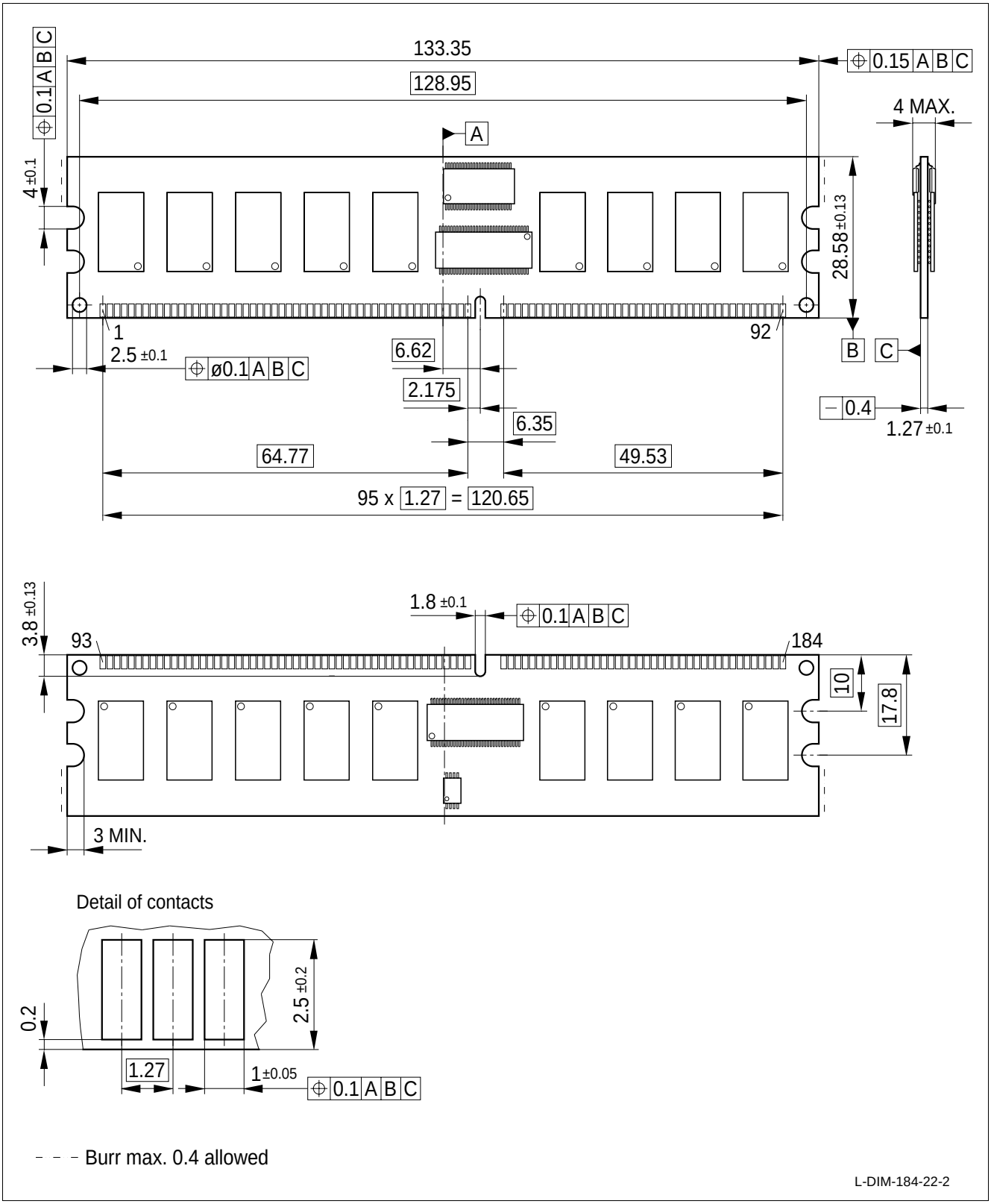


Figure 4 Package Outline – Raw Card C DDR Registered DIMM HYS72D128300GBR–[5/6/7]–B

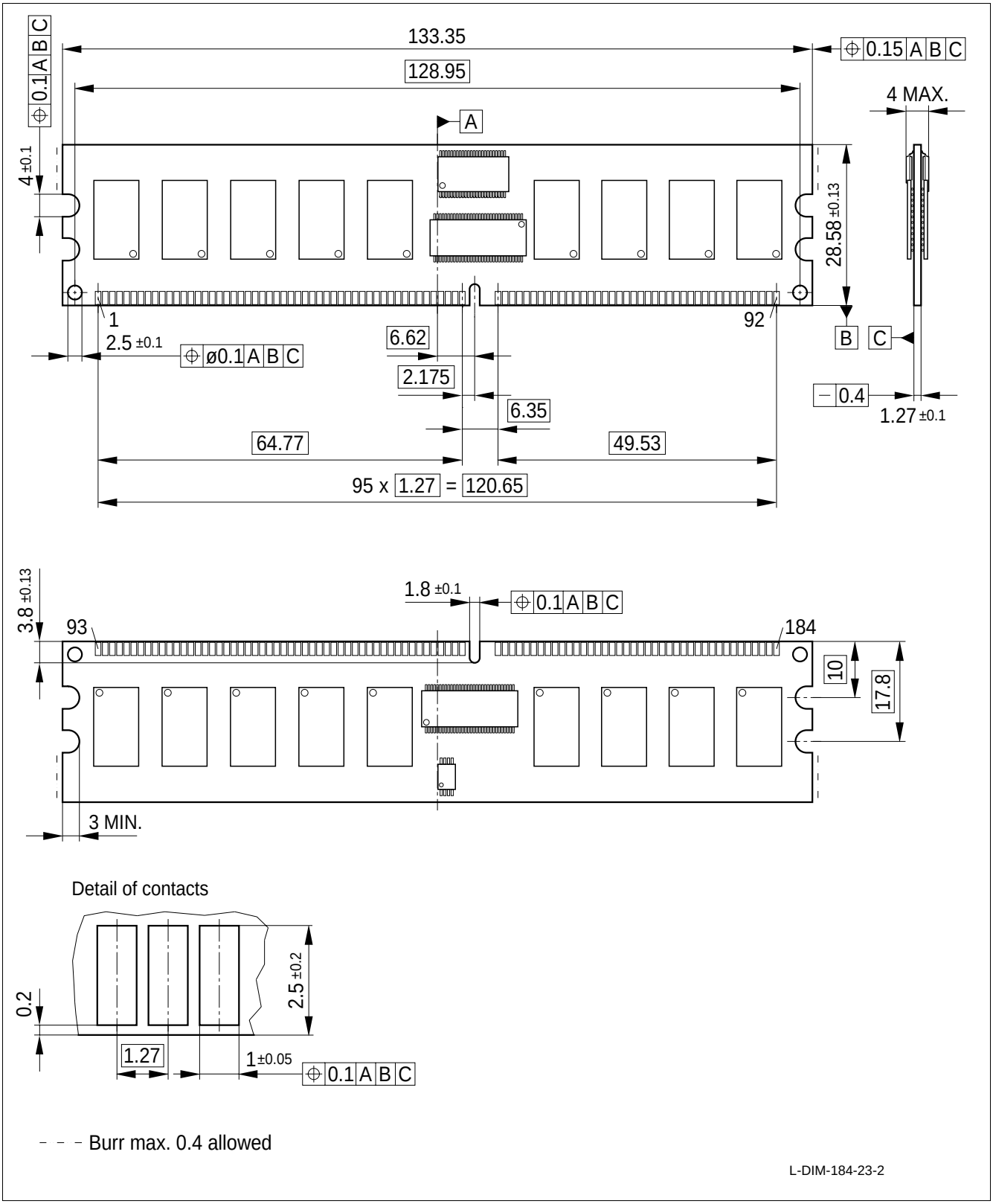


Figure 5 Package Outline – Raw Card B DDR Registered DIMM HYS72D128321HR–[5/6/7]–B

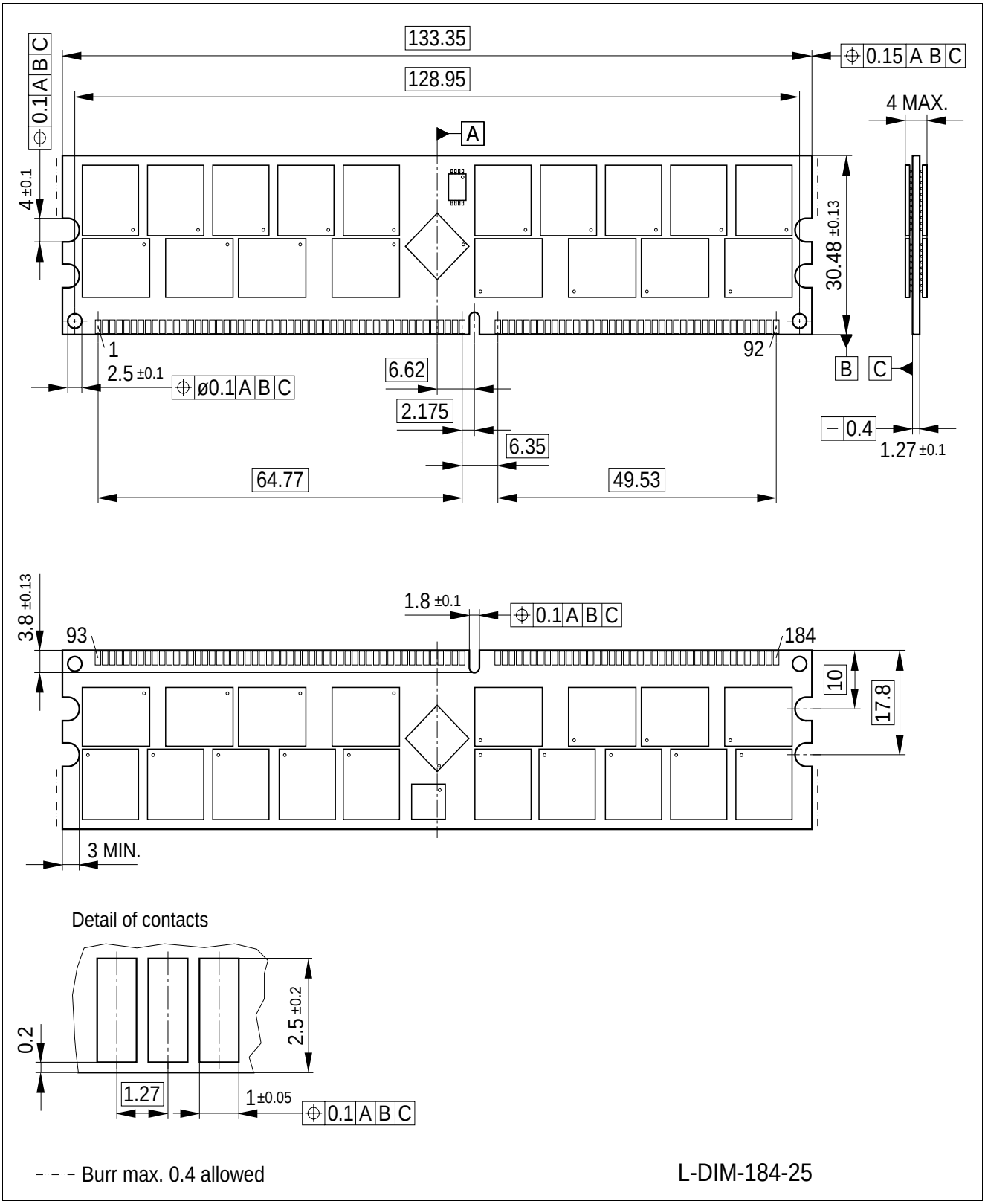


Figure 6 Package Outline – Raw Card D DDR Registered DIMM HYS72D256320GBR–[5/6/7]–B

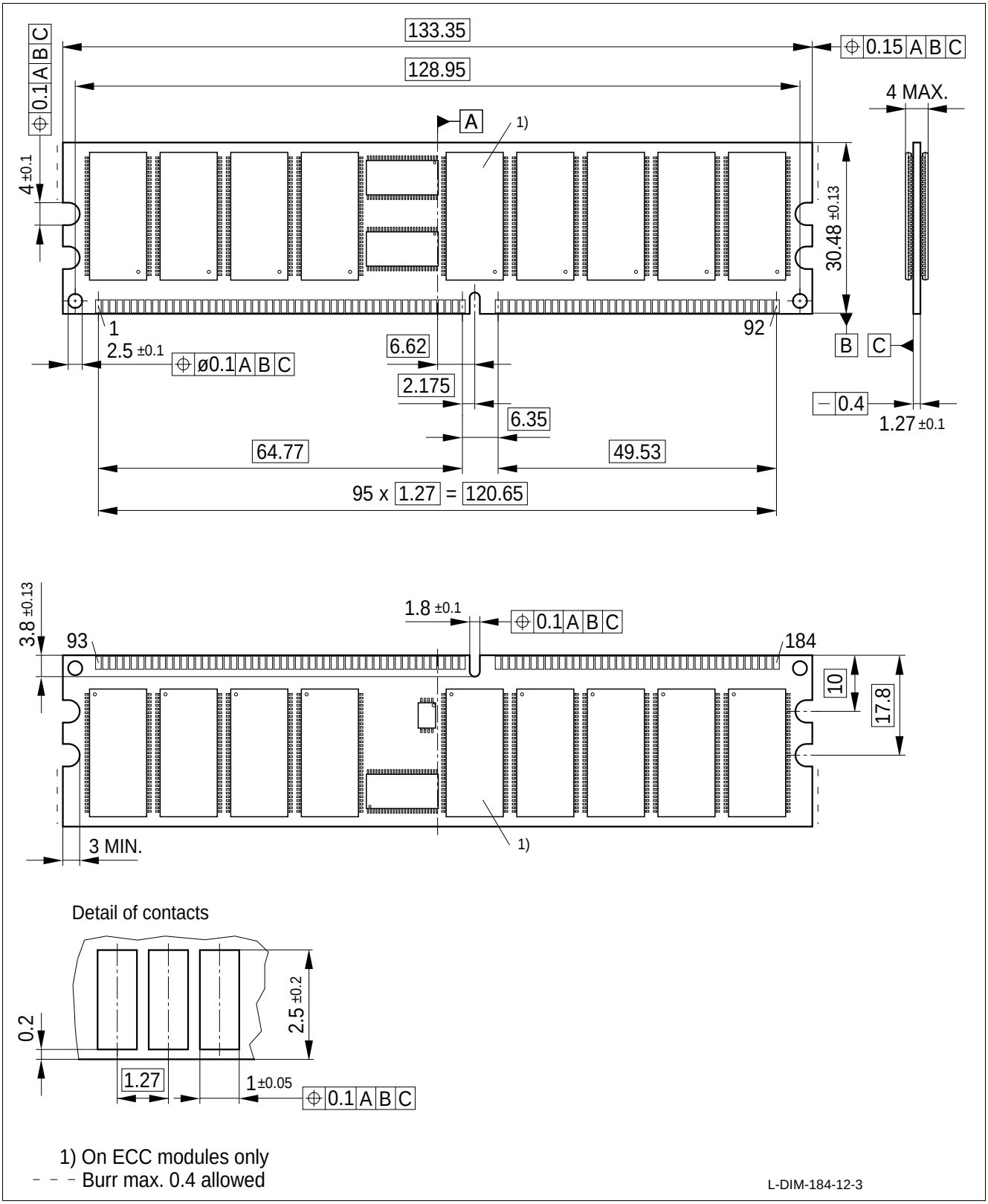


Figure 7 Package Outline – Raw Card M DDR Registered DIMM HYS72D128500HR–[7/7F]–B

6 Application Note

Power Up and Power Management on DDR Registered DIMMs

(according to JEDEC ballot JC-42.5 Item 1173)

184-pin Double Data Rate (DDR) Registered DIMMs include two new features to facilitate controlled power-up and to minimize power consumption during low power mode. One feature is externally controlled via a system-generated RESET signal; the second is based on module detection of the input clocks. These enhancements permit the modules to power up with SDRAM outputs in a High-Z state (eliminating risk of high current dissipations and/or dotted I/Os), and result in the powering-down of module support devices (registers and Phase-Locked Loop) when the memory is in Self-Refresh mode.

The new RESET pin controls power dissipation on the module's registers and ensures that CKE and other SDRAM inputs are maintained at a valid 'low' level during power-up and self refresh. When RESET is at a low level, all the register outputs are forced to a low level, and all differential register input receivers are powered down, resulting in very low register power consumption. The $\overline{\text{RESET}}$ pin, located on DIMM tab #10, is driven from the system as an asynchronous signal according to the attached details. Using this function also permits the system and DIMM clocks to be stopped during memory Self Refresh operation, while ensuring that the SDRAMs stay in Self Refresh mode.

Table 18 The function for $\overline{\text{RESET}}$ is as follows:[1)]

Register Inputs				Register Outputs
RESET	CK	CK	Data in (D)	Data out (Q)
H	Rising	Falling	H	H
H	Rising	Falling	L	L
H	L or H	L or H	X	Qo
H	High Z	High Z	X	Illegal input conditions
L	X or Hi-Z	X or Hi-Z	X or Hi-Z	L

1) X : Don't care, Hi-Z : High Impedance, Qo: Data latched at the previous of CK risning and CK falling

As described in the table above, a low on the $\overline{\text{RESET}}$ input ensures that the Clock Enable (CKE) signal(s) are maintained low at the SDRAM pins (CKE being one of the 'Q' signals at the register output). Holding CKE low maintains a high impedance state on the SDRAM DQ, DQS and DM outputs — where they will remain until activated by a valid 'read' cycle. CKE low also maintains SDRAMs in Self Refresh mode when applicable.

The DDR PLL devices automatically detect clock activity above 20MHz. When an input clock frequency of 20MHz or greater is detected, the PLL begins operation and initiates clock frequency lock (the minimum operating frequency at which all specifications will be met is 95MHz). If the clock input frequency drops below 20MHz (actual detect frequency will vary by vendor), the PLL VCO (Voltage Controlled Oscillator) is stopped, outputs are made High-Z, and the differential inputs are powered down — resulting in a total PLL current consumption of less than 1mA. Use of this low power PLL function makes the use of the PLL $\overline{\text{RESET}}$ (or $\overline{\text{G}}$ pin) unnecessary, and it is tied inactive on the DIMM.

This application note describes the required and optional system sequences associated with the DDR Registered DIMM '$\overline{\text{RESET}}$' function. It is important to note that all references to CKE refer to both CKE0 and CKE1 for a 2-bank DIMM. Because $\overline{\text{RESET}}$ applies to all DIMM register devices, it is therefore not possible to uniquely control CKE to one physical DIMM bank through the use of the $\overline{\text{RESET}}$ pin.

Power-Up Sequence with $\overline{\text{RESET}}$ — Required

1. The system sets $\overline{\text{RESET}}$ at a valid low level. This is the preferred default state during power-up. This input condition forces all register outputs to a low state independent of the condition on the register inputs (data and clock), ensuring that CKE is at a stable low-level at the DDR SDRAMs.
2. *The power supplies should be initialized according to the JEDEC-approved initialization sequence for DDR SDRAMs.*
3. Stabilization of Clocks to the SDRAM The system must drive clocks to the application frequency (PLL operation is not assured until the input clock reaches 20MHz). Stability of clocks at the SDRAMs will be affected by all applicable system clock devices, and time must be allotted to permit all clock devices to settle. Once a stable clock is received at the DIMM PLL, the required PLL stabilization time (assuming power to the DIMM is stable) is 100 microseconds. When a stable clock is present at the SDRAM input (driven from the PLL), the DDR SDRAM requires 200 µsec prior to SDRAM operation.
4. The system applies valid logic levels to the data inputs of the register (address and controls at the DIMM connector). CKE must be maintained low and all other inputs should be driven to a known state. In general these commands can be determined by the system designer. One option is to apply an SDRAM 'NOP' command (with CKE low), as this is the first command defined by the JEDEC initialization sequence (ideally this would be a 'NOP Deselect' command). A second option is to apply low levels on all of the register inputs to be consistent with the state of the register outputs.
5. The system switches $\overline{\text{RESET}}$ to a logic 'high' level. The SDRAM is now functional and prepared to receive commands. Since the $\overline{\text{RESET}}$ signal is asynchronous, setting the $\overline{\text{RESET}}$ timing in relation to a specific clock edge is not required (during this period, register inputs must remain stable).
6. The system must maintain stable register inputs until normal register operation is attained. The registers have an activation time that allows their clock receivers, data input receivers, and output drivers sufficient time to be turned on and become stable. During this time the system must maintain the valid logic levels described in step 5. It is also a functional requirement that the registers maintain a low state at the CKE outputs to guarantee that the DDR SDRAMs continue to receive a low level on CKE. Register activation time (t (ACT)), from asynchronous switching of $\overline{\text{RESET}}$ from low to high until the registers are stable and ready to accept an input signal, is specified in the register and DIMM do-umentation.
7. The system can begin the JEDEC-defined DDR SDRAM power-up sequence (according to the JEDEC-pproved initialization sequence).

Self Refresh Entry ($\overline{\text{RESET}}$ low, clocks powered off) — Optional

Self Refresh can be used to retain data in DDR SDRAM DIMMs even if the rest of the system is powered down and the clocks are off. This mode allows the DDR SDRAMs on the DIMM to retain data without external clocking. Self Refresh mode is an ideal time to utilize the $\overline{\text{RESET}}$ pin, as this can reduce register power consumption ($\overline{\text{RESET}}$ low deactivates register CK and CK, data input receivers, and data output drivers).

1. The system applies Self Refresh entry command. (CKE→Low, $\overline{\text{CS}}$→Low, $\overline{\text{RAS}}$ → Low, $\overline{\text{CAS}}$→ Low, $\overline{\text{WE}}$→ High)

Note: Note: The commands reach the DDR SDRAM one clock later due to the additional register pipelining on a Registered DIMM. After this command is issued to the SDRAM, all of the address and control and clock input conditions to the SDRAM are Don't Cares— with the exception of CKE.

2. The system sets $\overline{\text{RESET}}$ at a valid low level. This input condition forces all register outputs to a low state, independent of the condition on the registerm inputs (data and clock), and ensures that CKE, and all other control and address signals, are a stable low-level at the DDR SDRAMs. Since the $\overline{\text{RESET}}$ signal is asynchronous, setting the $\overline{\text{RESET}}$ timing in relation to a specific clock edge is not required.
3. The system turns off clock inputs to the DIMM. (Optional)
   a. In order to reduce DIMM PLL current, the clock inputs to the DIMM are turned off, resulting in High-Z clock inputs to both the SDRAMs and the registers. This must be done after the $\overline{\text{RESET}}$ deactivate time of the register (t (INACT)). The deactivate time defines the time in which the clocks and the control and address

signals must maintain valid levels after $\overline{\text{RESET}}$ low has been applied and is specified in the register and DIMM documentation.

b. The system may release DIMM address and control inputs to High-Z. This can be done after the RESET deactivate time of the register. The deactivate time defines the time in which the clocks and the control and the address signals must maintain valid levels after RESET low has been applied. It is highly recommended that CKE continue to remain low during this operation.

4. The DIMM is in lowest power Self Refresh mode.

Self Refresh Exit ($\overline{\text{RESET}}$ low, clocks powered off) — Optional

1. Stabilization of Clocks to the SDRAM. The system must drive clocks to the application frequency (PLL operation is not assured until the input clock reaches ~20MHz). Stability of clocks at the SDRAMs will be affected by all applicable system clock devices, and time must be allotted to permit all clock devices to settle. Once a stable clock is received at the DIMM PLL, the required PLL stabilization time (assuming power to the DIMM is stable) is 100 microseconds.
2. The system applies valid logic levels to the data inputs of the register (address and controls at the DIMM connector). CKE must be maintained low and all other inputs should be driven to a known state. In general these commands can be determined by the system designer. One option is to apply an SDRAM ‘NOP’ command (with CKE low), as this is the first command defined by the JEDEC Self Refresh Exit sequence (ideally this would be a ‘NOP Deselect’ command). A second option is to apply low levels on all of the register inputs, to be consistent with the state of the register outputs.
3. The system switches $\overline{\text{RESET}}$ to a logic ‘high’ level. The SDRAM is now functional and prepared to receive commands. Since the $\overline{\text{RESET}}$ signal is asynchronous, $\overline{\text{RESET}}$ timing relationship to a specific clock edge is not required (during this period, register inputs must remain stable).
4. The system must maintain stable register inputs until normal register operation is attained. The registers have an activation time that allows the clock receivers, input receivers, and output drivers sufficient time to be turned on and become stable. During this time the system must maintain the valid logic levels described in Step 2. It is also a functional requirement that the registers maintain a low state at the CKE outputs to guarantee that the DDR SDRAMs continue to receive a low level on CKE. Register activation time (t (ACT)), from asynchronous switching of $\overline{\text{RESET}}$ from low to high until the registers are stable and ready to accept an input signal, is specified in the register and DIMM do-umentation.
5. System can begin the JEDEC-defined DDR SDRAM Self Refresh Exit Procedure.

Self Refresh Entry ($\overline{\text{RESET}}$ low, clocks running) — Optional

Although keeping the clocks running increases power consumption from the on-DIMM PLL during self refresh, this is an alternate operating mode for these DIMMs.

1. System enters Self Refresh entry command. (CKE→ Low, $\overline{\text{CS}}$→ Low, $\overline{\text{RAS}}$→ Low, $\overline{\text{CAS}}$→ Low, $\overline{\text{WE}}$→ High)

Note: Note: The commands reach the DDR SDRAM one clock later due to the additional register pipelining on a Registered DIMM. After this command is issued to the SDRAM, all of the address and control and clock input conditions to the SDRAM are Don’t Cares — with the exception of CKE.

2. The system sets $\overline{\text{RESET}}$ at a valid low level. This input condition forces all register outputs to a low state, independent of the condition on the data and clock register inputs, and ensures that CKE is a stable low-level at the DDR SDRAMs.
3. The system may release DIMM address and control inputs to High-Z. This can be done after the $\overline{\text{RESET}}$ deactivate time of the register (t (INACT)). The deactivate time describes the time in which the clocks and the control and the address signals must maintain valid levels after $\overline{\text{RESET}}$ low has been applied. It is highly recommended that CKE continue to remain low during the operation.
4. The DIMM is in a low power, Self Refresh mode.

Self Refresh Exit ($\overline{\text{RESET}}$ low, clocks running) — Optional

1. The system applies valid logic levels to the data inputs of the register (address and controls at the DIMM connector). CKE must be maintained low and all other inputs should be driven to a known state. In general these commands can be determined by the system designer. One option is to apply an SDRAM 'NOP' command (with CKE low), as this is the first command defined by the Self Refresh Exit sequence (ideally this would be a 'NOP Deselect' command). A second option is to apply low levels on all of the register inputs to be consistent with the state of the register outputs.
2. The system switches $\overline{\text{RESET}}$ to a logic 'high' level. The SDRAM is now functional and prepared to receive commands. Since the $\overline{\text{RESET}}$ signal is asynchronous, it does not need to be tied to a particular clock edge (during this period, register inputs must continue to remain stable).
3. The system must maintain stable register inputs until normal register operation is attained. The registers have an activation time that allows the clock receivers, input receivers, and output drivers sufficient time to be turned on and become stable. During this time the system must maintain the valid logic levels described in Step 1. It is also a functional requirement that the registers maintain a low state at the CKE outputs in order to guarantee that the DDR SDRAMs continue to receive a low level on CKE. This activation time, from asynchronous switching of $\overline{\text{RESET}}$ from low to high, until the registers are stable and ready to accept an input signal, is t (ACT) as specified in the register and DIMM documentation.
4. The system can begin JEDEC defined DDR SDRAM Self Refresh Exit Procedure.

Self Refresh Entry/Exit ($\overline{\text{RESET}}$ high, clocks running) — Optional

As this sequence does not involve the use of the $\overline{\text{RESET}}$ function, the JEDEC standard SDRAM specification explains in detail the method for entering and exiting Self Refresh for this case.

Self Refresh Entry ($\overline{\text{RESET}}$ high, clocks powered off) — Not Permissible

In order to maintain a valid low level on the register output, it is required that either the clocks be running and the system drive a low level on CKE, or the clocks are powered off and $\overline{\text{RESET}}$ is asserted low according to the sequence defined in this application note. In the case where $\overline{\text{RESET}}$ remains high and the clocks are powered off, the PLL drives a High-Z clock input into the register clock input. Without the low level on $\overline{\text{RESET}}$ an unknown DIMM state will result.

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